

REMARKS

(1) Claims 1-9, 11-13, and 22-34 are pending in the present application.

(2) The Office Action cited the following references:

A. U. S. Patent 6,313,024 B1, by Cave, *et al.*, entitled *Method For Forming A Semiconductor Device* (referred to as "Cave" hereinafter);

B. U. S. Patent 6,261,944 B1, by Mehta, *et al.*, entitled *Method For Forming A Semiconductor Device Having High Reliability Passivation Overlying A Multi-Level Interconnect* (referred to as "Mehta" hereinafter);

C. U. S. Patent Application 2001/0045651 A1, by Saito, *et al.*, entitled *Semiconductor Integrated Circuit Device And A Method Of Manufacturing The Same* (referred to as "Saito" hereinafter);

D. U.S. Patent 6,022,809 by Fan, entitled *Composite Shadow Ring For An Etch Chamber And Method Of Using* (referred to as "Fan" hereinafter); and

E. U.S. Patent 5,075,965 by Carey, *et al.*, Entitled *Low Temperature Controlled Collapse Chip Attach Process* (referred to as "Carey" herein after).

(3) Claims 12-13 and 34 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave in view of Metha. Claims 22-26 and 28 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave in view of Saito. Claims 1 and 6-9 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave in view of Saito, and further in view of Mehta. Claims 2-5, 11, and 29-33 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave in view of Mehta, Saito, or Saito and Mehta, and further in view of Fan. Claim 27 was rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave in view Saito, and further in view of Carey. Applicant respectfully traverses these rejections for the following reasons.

Regarding obviousness, MPEP 2143 (8th ed., rev. 2, May 2004) states:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Claims 1-9 and 22-28

None of the cited references, either alone or in combination, disclose, teach, suggest, or motivate a method of forming a post passivation interconnect (PPI) structure as claims 1-9 and 22-28 require. The Office Action states that Cave “fails to disclose expressly the first plurality of contact pads could otherwise be used to provide electrical connection to an external component in packaging the integrated circuit by the formation of wire bonds or solder balls on the first plurality of contact pads.” The Office Action relies on newly cited Saito for teaching this limitation.

But as with the other cited references, Saito merely shows conventional metal interconnects leading up to a single set of contact pads (one connection pattern). Saito and the other cited references do not disclose, teach, or suggest a post passivation interconnect (PPI) structure having a second connection pattern that differs from a first connection pattern, where the first connection pattern includes a first plurality of contact pads that could otherwise be used to provide electrical connection to an external component in packaging the integrated circuit by the formation of wire bonds or solder balls on the first plurality of contact pads, and where the second connection pattern includes a second plurality of contact pads.

The Office action has failed to show how any of the cited references, singularly or combined, disclose, teach, suggest, or motivate such a structure. Thus, Cave and Saito cannot be combined to provide the PPI structure required by claims 22-26 and 28. Regarding claims 1-9, Cave and Saito provide no foundation for combination with Mehta. And regarding claim 27, Cave and Saito provide no foundation for combination with Carey.

Accordingly, Applicant respectfully asserts that claims 1-9 and 22-28 are patentable over the cited references. If the rejection of claims 1-9 and 22-28 should be maintained, it is respectfully requested that the Patent Office point out with particularity how and where the cited references, either singularly or combined, disclose, teach, or suggest *all the claim limitations* of claims 1-9 and 22-28. In the absence of a *prima facie* showing of obviousness by the Patent Office, Applicant submits that claims 1-9 and 22-28 should now be allowed.

Claims 11-13, 29-33, and 34

None of the cited references, either alone or in combination, disclose, teach, suggest, or motivate a method of forming a post passivation interconnect (PPI) structure over a substantially complete integrated circuit, as claims 11-13, 29-33, and 34 require.

The term "substantially complete integrated circuit" is defined and described in the patent specification. For example, while describing an illustrative embodiment (see e.g., FIGs. 1- 3b) of the present invention, paragraph [0022] provides: "Passivation layer 18 is the topmost layer of integrated circuit 10. This layer is formed after the circuitry of integrated circuit 10 is substantially complete. In other words, the circuits of the device are fully interconnected and operational when the passivation layer 18 is formed. The only remaining step is to provide access to power, ground and other signals so that the device can be coupled to other components." As another example, while describing an illustrative embodiment (see e.g., FIGs. 1-3b) of the present invention, paragraph [0034] provides: "The process begins with a substantially completed integrated circuit as shown in FIG. 1. In this context, a substantially completed integrated circuit is an integrated circuit that has been formed to the point that only connection to outside circuits is necessary to allow the device to operate as designed."

The cited references merely show conventional metal interconnects leading up to a single set of contact pads (one connection pattern), not a PPI structure. Accordingly, Applicant respectfully asserts that claims 11-13, 29-33, and 34 are patentable over the cited references.

If the rejection of claims 11-13, 29-33, and 34 should be maintained, it is respectfully requested that the Patent Office point out with particularity how and where the cited references, either singularly or combined, disclose, teach, or suggest *all the claim limitations* of

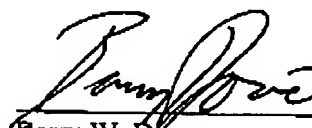
claims 11-13, 29-33, and 34. In the absence of a *prima facie* showing of obviousness by the Patent Office, Applicant submits that claims 11-13, 29-33, and 34 should now be allowed.

(4) In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the case be passed to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at the address below. No fees are due at this time. In the event that there are indeed fees due herein that are needed to keep the application pending, other than an issue fee, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date



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